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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/735,560	12/12/2003	Nara Won	TI-35878	3936

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TEXAS INSTRUMENTS INCORPORATED
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EXAMINER	
LEE, JOHN J	

ART UNIT	PAPER NUMBER
2618	

NOTIFICATION DATE	DELIVERY MODE
09/09/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/735,560	WON, NARA	
	Examiner	Art Unit	
	JOHN J. LEE	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24,25,28-33,35 and 36* is/are rejected.

7)☒ Claim(s) *26,27,34 and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claims 24, 25, 28-33, 35, and 36** are rejected under 35 U.S.C. 103(a) as being unpatentable over Briancon et al. (US 7,163,155) in view of Hayashi et al. (US 2004/0102176).

Regarding **claim 24**, Briancon teaches an integrated circuit board (Fig. 13). Briancon teaches that a multiplicity of semiconductor chips (Fig. 1, 2) for processing signal groups (Fig. 1, 2), wherein a plurality of semiconductor chips exchange signal groups using wireless techniques (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62). Briancon teaches that the multiplicity of semiconductor chips (Fig. 13) including a first semiconductor chip (Fig. 1) on the circuit board operable to receive a signal group (column 2, lines 55 – column 3, lines 29 and Fig. 1) from a second semiconductor chip (Fig. 2) on the circuit board (Fig. 1, 13, column 3, lines 18 – 29, and column 2, lines 55 – column 3, lines 29). Briancon teaches that the first semiconductor chip (Fig. 1) having an antenna (16) for receiving wireless signals transmitted from the second semiconductor chip (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62). Briancon teaches that a wireless signal receiver coupled to the antenna (16), the receiver operable to

detect the wireless signals (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62).

Briancon does not specifically disclose the limitation "a demodulator coupled to the receiver, the demodulator operable to recover the signal group from the wireless signals". However, Hayashi teaches the limitation "a demodulator (212a, 212b) coupled to the receiver, the demodulator operable to recover the signal group from the wireless signals" (Fig. 4 and pages 4, paragraphs 50 – 54). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Briancon's system as taught by Hayashi, provide the motivation to achieve enhancing reception signal for quality output in integrated circuit.

Regarding **claim 25**, Briancon does not specifically disclose the limitation "signals received by the wireless signal receiver are modulated with a modulation from the group consisting of amplitude modulation and frequency modulation". However, Hayashi teaches the limitation "signals received by the wireless signal receiver are modulated with a modulation from the group consisting of amplitude modulation and frequency modulation" (Fig. 4 and page 1, paragraphs 1 – 9). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Briancon's system as taught by Hayashi, provide the motivation to achieve enhancing tuning reception signal in order to provide selecting desired band in integrated circuit.

Regarding **claim 28**, Briancon and Hayashi teach all the limitation as discussed in claim 24. Furthermore, Briancon teaches that modulating and

transmitting a wireless signal by a first semiconductor chip (column 2, lines 55 – column 3, lines 29 and Fig. 1), the wireless signal being modulated with a logic signal group generated by the first semiconductor chip (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62). Briancon teaches that receiving and the wireless signal by a second semiconductor chip (column 2, lines 55 – column 3, lines 29, Fig. 1) to reproduce the logic signal group for use by the second semiconductor chip (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62).

Regarding **claim 29**, Briancon and Hayashi teach all the limitation as discussed in claim 24. Furthermore, Briancon teaches that the wireless signal transmits signal groups formatted in a serial format (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62).

Regarding **claim 30**, Briancon and Hayashi teach all the limitation as discussed in claims 24 and 25.

Regarding **claim 31**, Briancon and Hayashi teach all the limitation as discussed in claim 24. Furthermore, Briancon teaches that the wireless signal comprises an encoded pattern of signals produced by the first semiconductor chip (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62).

Regarding **claim 32**, Briancon does not specifically disclose the limitation "the receiving and demodulating of the wireless signal provide a decoded signal representing the pattern of signals produced by the first semiconductor chip". However, Hayashi teaches the limitation "the receiving and demodulating (212a, 212b) of the wireless signal provide a decoded signal representing the pattern of signals produced by the first semiconductor chip (Fig. 1)" (Fig. 4 and pages 4,

paragraphs 50 – 54). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the Briancon's system as taught by Hayashi, provide the motivation to achieve enhancing reception signal for quality output in integrated circuit.

Regarding **claim 33**, Briancon and Hayashi teach all the limitation as discussed in claim 24. Furthermore, Briancon teaches that a first semiconductor chip (Fig. 1) comprising a first processing unit (17), and a wireless transmitting unit (16) coupled to the first processing unit (column 2, lines 55 – column 3, lines 29 and Fig. 1) and operable to receive a signal group therefrom (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62). Briancon teaches that the wireless transmitting unit coupled to an antenna (16) within the first semiconductor chip and operable to transmit the signal group from the first processing unit (17) (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62). Briancon teaches that a second semiconductor chip (Fig. 2) located in close proximity to the first semiconductor chip (Fig. 13), the second semiconductor chip (Fig. 2) comprising a second processing unit (control logic circuitry) (Fig. 2) and a wireless receiving unit coupled to the second processing unit (column 2, lines 55 – column 3, lines 67 and Fig. 2), the wireless receiving unit coupled to an antenna within the second semiconductor chip (Fig. 12, 13 and column 7, lines 59 – column 8, lines 62) and operable to receive the signal group from the transmitting unit and to provide the signal group to the second processing unit (column 3, lines 18 – column 4, lines 59 and Fig. 2).

Regarding **claim 35**, Briancon and Hayashi teach all the limitation as discussed in claims 24 and 28. Furthermore, Briancon teaches that the first semiconductor chip is located on a first circuit board and the second semiconductor chip is located on a second circuit board (Fig. 9, 10), the first circuit board and the second circuit board being in a stacked configuration in close proximity (Fig. 9, 13 and column 7, lines 38 – column 8, lines 62).

Regarding **claim 36**, Briancon and Hayashi teach all the limitation as discussed in claims 24 and 28. Furthermore, Briancon teaches that the first semiconductor chip and the second semiconductor chip are positioned on a same board (Fig. 13 and column 7, lines 38 – column 8, lines 62).

Allowable Subject Matter

3. Claims 26, 27, 34, and 37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose the limitation "the first semiconductor chip includes an analyzer and a synthesizer, the analyzer operable to receive the signal group from the demodulator and to decode the signal group into a plurality of logic signals, and the second semiconductor chip comprises an analyzer for processing a serially transmitted signal group, and the wireless signals include a header portion, a data portion, and a tail portion" as specified the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Irie et al. (US 2006/0293004) discloses Semiconductor Integrated Circuit Device and Wireless Communication System.

Information regarding...Patent Application Information Retrieval (PAIR) system... at 866-217-9197 (toll-free)."

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231
Or P.O. Box 1450
Alexandria VA 22313

or faxed (571) 273-8300, (for formal communications intended for entry)

Or: (703) 308-6606 (for informal or draft communications, please label "PROPOSED" or "DRAFT").

Hand-delivered responses should be brought to USPTO Headquarters, Alexandria, VA.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to **John J. Lee** whose telephone number is **(571) 272-7880**. He can normally be reached Monday-Thursday and alternate Fridays from 8:30am-5:00 pm. If attempts to reach the examiner are unsuccessful, the examiner's supervisor, **Nay Maung**, can be reached on **(571) 272-7882**. Any

inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-4700.

J.L
September 1, 2008

John J Lee

/JOHN J LEE/
Primary Examiner, Art Unit 2618